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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,845	11/25/2003	Brian J. McNamara	00P 7673 US 02	8177
26181	7590	06/15/2005	EXAMINER	
FISH & RICHARDSON P.C. PO BOX 1022 MINNEAPOLIS, MN 55440-1022			LY, NGH I H	
			ART UNIT	PAPER NUMBER
			2686	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/722,845

Applicant(s)

MCNAMARA ET AL.

Examiner

Nghi H. Ly

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 27 and 28 have been renumbered 26 and 27, respectively.

Double Patenting

2. Claims 13-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-11 of McNamara et al, U.S. Patent No. 6,665,528. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claims 13, 21 and 22, McNamara teaches a dual band mixer (see column 4, line 31 to column 6, lines 26), comprising: a first transistor to mix a first local oscillator input signal with a first radio frequency input signal (see column 4, line 31 to column 6, lines 26), a second transistor to mix a second local oscillator input signal with a second radio frequency input signal, the second radio frequency input signal operating at a different radio frequency band than the first radio frequency input signal (see column 4, line 31 to column 6, lines 26), a common node for at least one of the first radio frequency input signal and the second radio frequency input signal and an

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intermediate frequency output-signal (also see column 4, line 31 to column 6, lines 26), wherein drains of the first and second transistors are coupled to the common node (also see column 4, line 31 to column 6, lines 26), and interconnection circuitry to turn off the second transistor when the first local oscillator input signal is applied to the first transistor and to turn off the first transistor when the second local oscillator input signal is applied to the second transistor (also see column 4, line 31 to column 6, lines 26).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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5. Claims 13-15, 17, 20-24, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobrovolny (US 5,280,648) in view of Li et al (US 5,678,226) and further in view of Irie (JP411205043A) and Franca-Neto (US 6,466,775).

Regarding claims 13, Dobrovolny teaches a dual band mixer (see Asbtract), comprising: a first transistor to mix a first local oscillator input signal with a first radio frequency input signal; a second transistor to mix a second local oscillator input signal with a second radio frequency input signal (see fig.1 a symmetric local oscillator LO connect with transistor 22 at gate G), and interconnection circuitry (see the S connection between two transistors 22 and 26).

Dobrovolny does not specifically disclose a common node for at least one of the first radio frequency input signal and the second radio frequency input signal and an intermediate frequency output signal, wherein drains of the first and second transistors are coupled to the common node.

Li teaches a common node (see fig.2, a node on the left side of C4) for at least one of the first radio frequency input signal (see fig.2, RF 18) and the second radio frequency input signal and an intermediate frequency output-signal (see fig.2, IF 20), wherein drains of the first and second transistors are coupled to the common node (see fig.2, the drain of transistor 12 connects with a node on the left side of C4).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to provide the above teaching of Li into the system of Dobrovolny so that circuit design can be simplified.

The combination of Dobrovolny and Li does not specifically disclose the second radio frequency input signal operating at a different radio frequency band than the first radio frequency input signal

Irie teaches the second radio frequency input signal operating at a different radio frequency band than the first radio frequency input signal (see Solution).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to provide the above teaching of Irie into the system of Dobrovolny and Li in order to suppress an interfering wave by an image frequency without accompanied increase in a circuit scale (see Irie, Problem to be solved).

The combination of Dobrovolny, Li and Irie does not specifically disclose interconnection circuitry to turn off the second transistor when the first local oscillator input signal is applied to the first transistor and to turn off the first transistor when the second local oscillator input signal is applied to the second transistor.

Franca-Neto teaches interconnection circuitry to turn off the second transistor when the first local oscillator input signal is applied to the first transistor and to turn off the first transistor when the second local oscillator input signal is applied to the second transistor (see column 5, lines 35-39).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to provide the above teaching of Franca-Neto into the system of Dobrovolny, Li and Irie in order to provide a highly linear and low voltage mixer (see Franca-Neto, Abstract).

Regarding claim 14, see the teaching of Li in claim 1 above.

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Regarding claim 15, Dobrovolny further teaches the first and second transistors are field effect transistors (Abstract, see "FET").

Regarding claim 17, Dobrovolny further teaches the interconnection circuitry includes a first network associated with the first transistor to generate a first negative voltage at a first node when the first local oscillator signal is applied to the gate of the first transistor and a second network associated with the second transistor to generate a second negative voltage at a second node when the second local oscillator signal is applied to the gate of the second transistor (see fig.2, LO 40 with negative and positive voltages).

Regarding claim 20, Dobrovolny further teaches a common line coupling the first and second nodes (see fig.2, the connection between two nodes under resistors 50 and 51).

Regarding claim 21, claim 21 is rejected with a similar reason as set forth in claim 13 above.

Regarding claim 22, claim 22 is rejected with a similar reason as set forth in claim 13 above.

Regarding claim 23, Dobrovolny further teaches the plurality of transistors each have source coupled to the ground (see fig.1, the source S of transistors 22 and 26 connect with ground).

Regarding claim 24, Dobrovolny further teaches the first and second transistors are field effect transistors (Abstract, see "FET").

Regarding claim 26, Dobrovolny further teaches the circuitry does not require an external voltage source (see fig.1).

Regarding claim 27, Dobrovolny further teaches generating a first negative voltage at a first node when the first local oscillator signal is applied to the gate of the first transistor (see fig.1 and fig.2, oscillator 40 and negative voltage), the first negative voltage to deactivate the second transistor, and generating a second negative voltage at a second node when the second local oscillator signal is applied to the gate of the second transistor, the second negative voltage to deactivate the first transistor (also see fig.1 and fig.2, oscillator 40 and negative voltage).

6. Claims 16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobrovolny (US 5,280,648) in view of Li et al (US 5,678,226) and further in view of Irie (JP411205043A), Franca-Neto (US 6,466,775) and Andrys et al (US 6,057,714).

Regarding claim 16, the combination of Dobrovolny, Li, Irie and Franca-Neto teaches claims 1 and 15. The combination of Dobrovolny, Li, Irie and Franca-Neto does not specifically disclose the first and second transistors are depletion-type transistors.

Andrys teaches the first and second transistors are depletion-type transistors (see column 4, lines 17-20).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to provide the above teaching of Andrys into the system of Dobrovolny, Li, Irie and Franca-Neto in order to provide balance on all ports in a communicating ring (see Andrys, column 4, lines 17-20).

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Regarding claim 25, claim 25 is rejected with a similar reason as set forth in claim 16 above.

7. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobrovolny (US 5,280,648) in view of Li et al (US 5,678,226) and further in view of Irie (JP411205043A), Franca-Neto (US 6,466,775) and Murtojarvi (US 5,678,224).

Regarding claim 18, the combination of Dobrovolny and Li teaches the mixer of claim 13. The combination of Dobrovolny and Li does not specifically disclose the first network includes a first diode connected between the gate of the first transistor and the first node, and a first capacitor and a second diode connected in parallel between the source of the first transistor and the first node.

Murtojarvi teaches the first network includes a first diode connected between the gate of the first transistor and the first node, and a first capacitor and a second diode connected in parallel between the source of the first transistor and the first node (see fig.2).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to provide the above teaching of Murtojarvi into the system of Dobrovolny, Li, Irie and Franca-Neto so that the leakage between the mixer outputs could have been minimized.

Regarding claim 19, claim 19 is rejected with a similar reason as set forth in claim 18 above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Mittel (US 5,630,228) teaches double balanced mixer circuit with active filter load for a portable communication receiver.

b. Kim (US 6,411,801) teaches double balanced active mixer.

c. Sano (US 5,884,154) teaches low noise mixer circuit having passive inductor elements.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghi H. Ly whose telephone number is (571) 272-7911. The examiner can normally be reached on 8:30 am-5:30 pm Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghi H. Ly

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